On the Effects of Hot Electrons on the DC and RF Characteristics of Lattice-Matched InAlAs/InGaAs/InP HEMT's

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***Abstract*—This letter for the first time presents results of hot electron stressing of InAlAs/InGaAs/InP high electron mobility transistors (HEMT's). High drain bias, room temperature stress cycles have been applied to 0.3 μm, SiN-passivated, lattice-matched devices, and the changes of the dc and rf (up to 50 GHz) characteristics have been studied. Both the dc and rf device gain degrade after stressing; the effect of the stress on the unity current gain cutoff frequency f_T is studied under different bias conditions. Results indicate that surface degradation may be responsible for the observed changes.**

I. Introduction

InP-BASED high electron mobility transistors (HEMT's) exhibit unparalleled performance in terms of gain and noise figure well into the millimeter-wave range, and a great deal of activity is presently being devoted to the understanding of their behavior [1], the development of ever better technologies [2], and the fabrication of both linear [3] and nonlinear [4] monolithic circuits for applications up to D-band. As a consequence of this growing interest, a few studies have been published in recent years on InP HEMT reliability, a key issue if a technology is to move out of the research labs and into the world of practical (if not commercial) applications. Researchers have so far concentrated on reliability testing using high-temperature accelerated stress [5]–[8], in one case with emphasis on the effect of the ambient gas [9]; since surface stability (together with metal contact degradation) was often identified as one of the most critical issues, different passivation techniques have been proposed for improved reliability [10]–[13].

This work for the first time reports on a different approach to the assessment of potential degradation mechanisms of InP HEMT's by focusing on the room temperature effects of hot electrons, a well-known concern due to the small channel bandgap and to the very short gates required for millimeter-wave operation. This means that if one wants to study the reliability hazards connected with hot electrons, the accelerating factor for device stress should not be the temperature, as in all of the works referenced above, but drain bias (i.e., channel longitudinal electric field). Due to enhanced lattice scattering, high temperatures are indeed known to inhibit electron heating. Such an approach has been recently applied to GaAs-based pseudomorphic HEMT's [14]–[16], but never to InP HEMT's. We thus believe that this work represents a timely and important contribution to the topic of InP-HEMT reliability, since room temperature stressing can isolate degradation mechanisms that may get masked by others (e.g., temperature activated phenomena like metal contact degradation) at higher temperatures.

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II. Experiments

We applied hot electron stress experiments to 0.3-μm δ-doped $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$/InP HEMT's designed and fabricated at IMEC [17], [18]. The devices, 100 μm wide, have a typical F_{min} of 1 dB with associated gain of 11 dB at 20 GHz. They are passivated by 200-nm-thick PECVD SiN, deposited in 25 min at 250° under growth conditions optimized for minimal stress (on 2-in. Si wafers a slightly compressive induced stress of $1.3 \cdot 10^8$ dyn/cm was measured); the index of refraction and dielectric constant were 1.86 and 7, respectively [19]. The effect of hot electrons on the device performance was evaluated by characterizing the samples at dc and rf on wafer before and after dc accelerated stress at high V_{DS}. Device characterization was performed up to the V_{DS} allowed by device specifications (3 V), and it did not induce any sort of device degradation. The characteristics obtained before the stress match the data measured at IMEC after processing within the small dispersion among devices of the same wafer. Moreover, unstressed devices have been measured at different times over several weeks showing excellent stability. Three devices have been stressed, all of them showing the same degradation mode. The stress sequence featured four steps at $V_{DS} = 4$ V, $V_{GS} = 0$ V, one at $V_{DS} = 4.25$ V, $V_{GS} = 0$ V, and one at $V_{DS} = 4.5$ V, $V_{GS} = 0$ V. The duration of each step was 30 min. All the experiments were done at room temperature. The presence of hot electrons and impact ionization under stress conditions is revealed by the typical bell shape of the gate current versus V_{GS} curve [16]. The observed device degradation, which is gradually enhanced by each subsequent step, is permanent, i.e., it was not recovered upon storing the devices at room temperature for a few months.

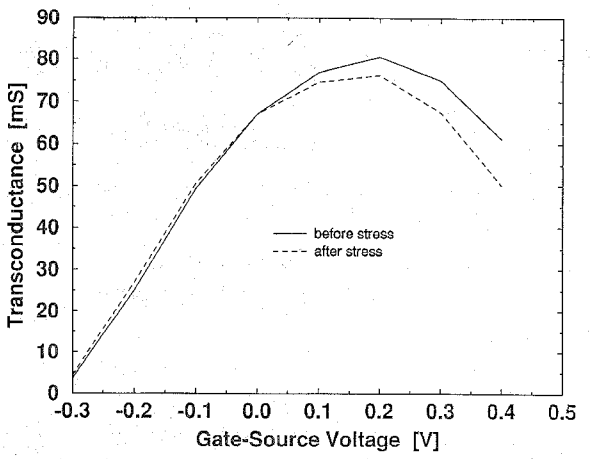

Fig. 1. Transconductance measured at $V_{DS} = 1$ V before and after a room temperature stress sequence featuring subsequent steps at $V_{DS} = 4$, 4.25, and 4.5 V; $V_{GS} = 0$ V during the stress, and the duration of each step is 30 min.

III. Results and Discussion

The only remarkable effect of the stress on the device dc characteristics is an I_{DS} decrease due to a transconductance compression at high V_{GS}, as illustrated by Fig. 1. The gate reverse current, due to both leakage and collection of holes generated in the channel by impact ionization, does not change significantly, indicating that the gate contact does not undergo appreciable degradation. Typical gate current values during the stress range between -30 and 50 μA. As to the rf behavior, we have measured the S-parameters up to 50 GHz using a HP-8510 network analyzer and a Cascade coplanar probe station. Fig. 2 shows the S-parameters of one of the devices under test, measured at $V_{GS} = 0.3$ V, $V_{DS} = 1$ V, both before and after the stress. The most important effect observed is a change of S_{21}, accompanied by a decrease of the magnitude of S_{22} that vanishes at high frequencies. The reduction of S_{21} reflects into a degradation of both the current gain (h_{21}) and the power gain (MSG, MAG); consequently, both f_T and $f_{\max}$ are degraded (at $V_{GS} = 0.3$ V, $V_{DS} = 1$ V, f_T decreases from 94–73 GHz, $f_{\max}$ from 100–80 GHz). The effect of the stress on the extrinsic f_T is reported in Fig. 3. As happens with g_m, at low V_{GS} the cutoff frequency is practically unchanged by the stress; as the gate bias increases, the f_T reduction becomes more and more severe. To compare the small-signal equivalent circuit parameters extracted before and after the stress, circuit optimization was done between 1 and 25 GHz using an in-house-developed genetic algorithm [20]. Since the shape of the g_m versus V_{GS} curve allows us to rule out any significant increase of source resistance (R_S) [6], we assumed that the device parasitics were not affected by the stress and kept them fixed at the pre-stress values. Modeled S-parameters, also reported in Fig. 2, show a very good match with measured data. The parameter values extracted at $V_{GS} = 0.3$ V, $V_{DS} = 1$ V indicate that the decrease of f_T is due to both a reduction of g_m (-16%) and an increase of C_{GS} (9%), while a drop of the intrinsic drain-source resistance R_{DS} (-15%) is responsible for the observed change of S_{22}.

From these results, and following the indications of [6], we may infer some information as to the degradation mechanism

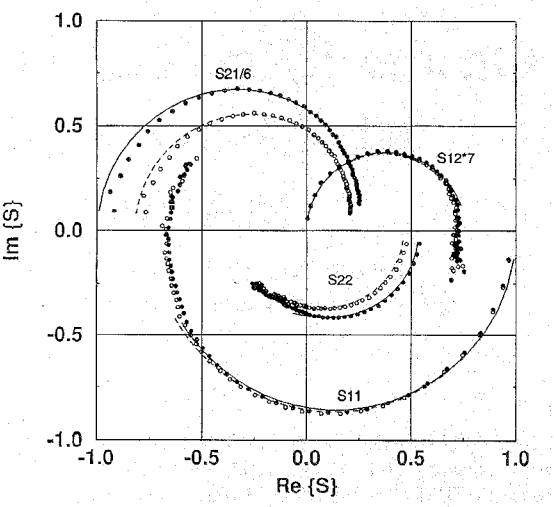

Fig. 2. S-parameters measured at $V_{GS} = 0.3$ V, $V_{DS} = 1$ V before (full circles) and after (open circles) the stress of Fig. 1. The frequency ranges from 1–50 GHz. Modeled data in the 1–25 GHz range are also shown (before stress: solid lines; after stress: dashed lines).

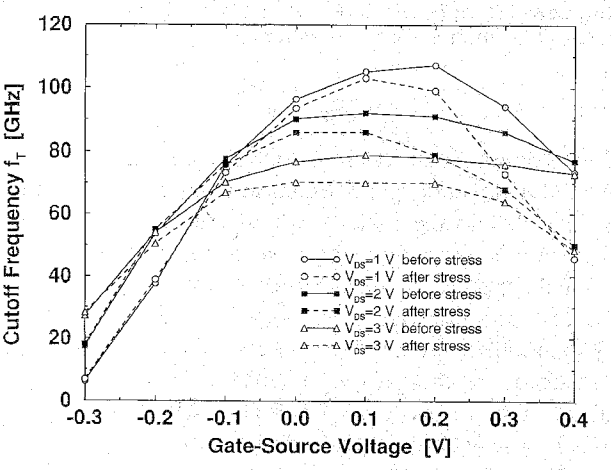

Fig. 3. Bias dependence of the unity current gain cutoff frequency f_T before and after the stress of Fig. 1.

brought about by the hot electron stress. To begin with, significant degradation of the gate contact can be ruled out, since 1) no horizontal shift (i.e., no change of the built-in potential) appears in the g_m curve of Fig. 1 and 2) the leakage remains practically unchanged. As previously noted, R_S cannot be held responsible for the decrease of g_m, because a change of R_S would show up at every bias point, which is contradicted by Fig. 1. Moreover, at the bias points chosen for device stress, the power dissipation is such that the thermal contribution to the degradation can be considered a minor one, therefore effects related with the lattice and 2DEG quality should not be an issue. On the other hand, the increase of the degradation with gate bias is generally encountered when the device surface is affected, since carrier transport takes place close to, and is more influenced by, the surface at high V_{GS}. That the device area affected by the stress is the passivation interface is further confirmed by the observation that the deposition of the SiN layer induces a change, namely an increase, of g_m in the same V_{GS} range where the hot electron degradation develops [19]. Surface degradation may

occur due to trap creation or charge capture at the interface between the semiconductor and the passivation, a commonly observed effect of hot electrons.

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